Proceedings of the 2nd European Microwave Integrated Circuits Conference

A 6W Uneven Doherty Power Amplifier in GaN Technology

A. Z. Markos [2], P. Colantonio[1], F. Giannini[1], R. Giofrè[1], M. Imbimbo[1], G. Kompa[2]

[1]*Univ. of Roma Tor Vergata, Dept. of Electronic Eng., Via del Politecnico 1, 00133 Roma Italy*
`paolo.colantonio@uniroma2.it`

[2]*Univ. of Kassel, Dept. of High Freq. Technique, Wilhelmshoeher Allee 73, D-34121 Kassel, Germany*
`zena@uni-kassel.de`

Abstract— **In this paper the design of a 6W uneven GaN Doherty power amplifier is presented. The Doherty PA is designed to achieve high efficiency for modulated signals with high peak to average power ratio used in modern wireless communication systems. The Doherty amplifier has been designed using two equal sized GaN devices for the Main Class AB and Peaking Class C amplifiers. An uneven power divider is used at the input to deliver more input power to the Peaking amplifier than the Main amplifier. The measured maximum output power of the realised uneven Doherty is 38 dBm with 60% of peak power added efficiency (76% of drain efficiency). The power added (drain) efficiency is higher than 52% (62%) up to 6 dB of back off, or 42% (45%) up to 10 dB of back off.**

I. INTRODUCTION

The power amplifiers (PAs) involved in the front end of communication systems are usually designed in Class AB mode, and operated in back-off conditions to fulfil the system linearity requirements. In modern wireless communication applications, signals with high dynamic range, e.g. high peak-to-average power ratio (PAR) are usually involved, in order to achieve high data rate transmission levels. For instance, in the UMTS standard with W-CDMA modulation, a PAR of 7-10 dB is typical, and higher values are expected for future standards. The high value of PAR implies a great back-off operating condition for the PA, leading to critical issues in achieving sufficiently high efficiency levels at the average output power. Nevertheless, simultaneous efficiency and linearity behaviour are becoming the relevant figures of merit to be considered in the design of high performance PA.

Unfortunately, it is well acclaimed that single ended PA is not sufficient to adequately achieve high average efficiency levels, while the linearity feature can be fulfilled adopting suitable external linearization schemes [1]. Consequently, different well known PA architectures, like the envelope elimination and restoration (EER), outphasing and Doherty have been extensively investigated [2].

Recently, many research efforts have been focused on the Doherty amplifier design technique [3], due to its relatively simple implementation and the resulting efficiency improvement advantages. Many of the designs reported are based on relatively matured device technologies, like GaAs [4] and LDMOS [5, 6] devices. However, there are only few published designs of Doherty amplifiers with the use of GaN devices [7].

The aim of this paper is to design, analyse and optimise an unevenly driven Doherty PA, based on GaN device, with the aim of improving the average efficiency in a suitable back-off range. In section II the basic principle of the Doherty PA will be reviewed, while the design of the uneven Doherty amplifier is discussed in section III. Realization and experimental results of the Doherty PA are also reported in section IV.

II. THE UNEVEN DOHERTY AMPLIFIER

The fundamental operating principle of the classical Doherty PA was already published in 1936 [3] and has been recently discussed in detail in [1]. Basically, the Doherty scheme uses two PAs combined in a suitable way to achieve and maintain a constant efficiency value for a fixed (usually 6 dB) range of the output power back off. The basic scheme of the Doherty amplifier, as depicted in Fig. 1, consists of a *Main* and a *Peaking* PA. At the beginning, only the Main PA is operating, while the Peaking PA is turned off, up to the achievement of its maximum efficiency. Then, the Peaking PA is turned on and used to control the modulation of the load seen by the Main PA.

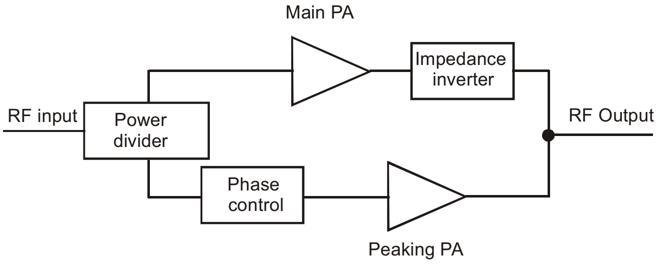
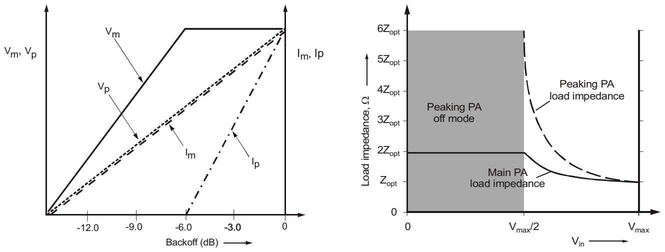


Fig. 1: Basic scheme of the Doherty PA.

Alternatively, the Doherty operation can be described by referring to the equivalent models for the two PAs. In particular, the Main PA starts to operate as a current source, with an impedance load two times as higher as its optimum load (R_{opt}). In this condition, the Main amplifier reaches a maximum output power half of its maximum ($0.5 \cdot P_{Main\_max}$) resulting also in its maximum efficiency value (e.g. 78% if ideal Class B bias condition). This point, referred as a breaking point, determines the turn-on of the Peaking amplifier. By exploiting the active load-pull principle [1], the load seen by the Main amplifier will now be theoretically modulated from $2R_{opt}$ to R_{opt}. During this phase, the Main PA acts as a voltage source, saturated to its maximum excursion, while its output current increases up to the maximum value. This dynamic load modulation keeps the Main PA efficiency theoretically constant, simultaneously preserving an elevated overall Doherty system efficiency, as analysed in [1]. The fundamental output voltages and currents of the Main and Peaking PAs, together with the ideal load modulation for both amplifiers, are shown in Fig. 2. The resulting theoretical efficiency of an ideal Doherty PA would be a constant efficiency maintained over the upper 6 dB power range.



(a) (b)

Fig. 2: Theoretical fundamental outputs voltages and currents of the Main and Peaking PAs (a) and load modulation (b).

The Doherty amplifier could be realized using Class B operating conditions for both the Main and Peaking amplifiers. However, in this case an additional control circuitry is required to turn on the Peaking amplifier only at the required input power level. Such additional control circuitry increases the complexity of the implementation, reducing the system overall efficiency. An alternative approach, adapted in many of the reported Doherty implementations [4-9], is based on the use of a Class C Peaking PA, in which its bias point is properly tuned to guarantee its activation at the proper input power level (e.g. at breaking point).

The main drawback in using Class C Peaking PA, is usually related to the necessity of a device able to attain higher output current level with respect to the one used for the Main PA, to provide the proper amount of current to fully modulate the load of the Main PA [1]. This issue can be easily solved, especially in monolithic design approach, by using two unequal sized devices for the Main and Peaking PA [8]. Conversely, in hybrid realization it could be difficult to attain the appropriate device scaling. Even though the use of adaptive biasing scheme for the Peaking PA is also proposed and implemented as a possible solution [9], the required additional circuitry reduces the simplicity of the Doherty design.

The other more feasible solution, proposed in [10], is based on the use of equal devices but uneven power splitting, thus delivering more RF input power to the Peaking PA rather than to the Main PA. Such different power splitting helps the Peaking amplifier to generate enough current so that proper load modulation is achieved. However, in this case additional optimisations are required to find the optimum load impedances for both the Peaking and the Main PAs, to achieve the proper load modulation. This uneven solution is also claimed to improve the linearity of the resulting Doherty amplifier, by avoiding the overdriving of the Main PA, as theoretically and experimentally reported in [10]. In this paper we demonstrate a Doherty amplifier through the use of two equal sized devices for the Main and Peaking PA design, exploiting uneven power drive and successive optimisation of bias points and output impedances for proper load modulation.

III. DOHERTY PA DESIGN

A 6W unevenly driven Doherty PA has been designed to operate at 2.1 GHz, and simulated using in-house large signal model of a 1 mm GaN HEMT device, provided by Selex SI, Italy. Since the final design is carried out gradually through optimisations, in the following the complete procedure to design the Doherty amplifier is explained step by step.

The Main PA is biased in a Class AB condition, resulting in V_{DS} =18V and V_{GS}=-4.4V (I_{DS}= 70 mA ≈ 10% of maximum drain current). The optimum impedance R_{opt} of the device for this class AB operation has been obtained from a tuned load design, obtaining the value R_{opt}=30Ω. Then the Main amplifier output network has been designed to operate the active device with half of its maximum output current at the breaking point, resulting in a 60Ω (2R_{opt}) of output impedance. The Main device matching network was designed accounting for the impedance transformation performed by the lambda-quarter line (see Fig. 1). The latter is a λ/4 line, with characteristic impedance equal to R_{opt} (30Ω), thus will invert the external load $R_{opt}/2$ to 2R_{opt}.

The Peaking PA has to be designed to operate in its full capacity, e.g. to reach the device maximum output current. The key point in the design of such amplifier is related to the suitable selection of the active device bias point for such a Class C amplifier. In fact, the Peaking device has to enter into its active region at the breaking point, which should result in 6 dB back-off with respect to the Doherty maximum output power.

Assuming for the moment the same input power splitting ratio for both Main and Peaking amplifiers, it follows that the Peaking device bias point should be chosen as the device pinch off voltage (-5.0V) decreased by the RF input voltage amplitude required to reach the breaking point of Main device (1.5V), thus resulting in V_{GS}=-6.5V. Then the output matching network of the Peaking amplifier has been designed, to synthesize the optimum load condition of 33Ω inferred for the device under such a nominal Class C operation. The complete Peaking amplifier comprises the input matching network and the additional λ/4 line, to compensate the phase delay introduced by the impedance inverter at the output of the Main PA (see Fig. 1).

Then, the Main and the Peaking PAs were combined and output matched to $R_{opt}/2$ (15Ω) starting from standard 50Ω, by using an additional λ/4 transmission line with characteristic impedance of 27.4Ω. The complete amplifier consists of bias and stabilising elements for both amplifiers.

Simulations have been performed to analyse the behaviour of this initial designed Doherty PA (note that at the moment the input power was divided evenly into the Main and Peaking PA). Most importantly, a wrong load modulation behaviour has been observed. This phenomena is confirmed by the load modulation curves reported in Fig. 3, from which it can be seen that due to inadequate amount of current from the Peaking PA, the load of the Main PA is not properly modulated (from 70Ω to 40Ω while it is expected to be modulated from 60Ω to 30Ω).

Therefore, it is obvious that this initial Doherty PA design requires an optimisation of the Peaking PA, with the aim to generate a higher current from the latter.

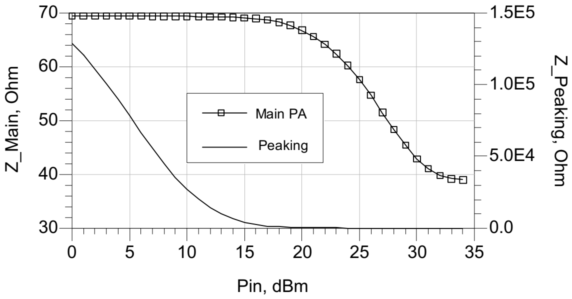


Fig. 3: Simulated load modulations of the Main and Peaking PA of the even Doherty design.

The next step was the identification of the suitable power splitting ratio (namely k) to design an uneven Doherty amplifier. The k factor, in terms of voltage ratio, was determined as the square ratio between the adopted gate bias voltages of the Main and Peaking PAs, resulting in k=0.67. Using this value for the input power splitting, the Main PA acquires 40% of the total input power, while the remaining is delivered to the Peaking PA.

This uneven power divider is based on a single section Wilkinson scheme, where the two $\lambda/4$ power dividing arms have different characteristics impedance [11].

The further optimisation criteria was to decrease the load impedance of the Peaking PA, to operate at its full capacity. This was performed by fine-tuning the Peaking output matching network. The 33Ω optimum impedance used in the first design was adjusted to 31.5Ω, to allow the maximum swing of the voltage for the Class C amplifier.

Finally, the Peaking PA bias point was adjusted to V_{GS}=-6.8V to maintain the breaking point at its original power level.

The resulting simulated load modulation for the Main and Peaking PAs are shown in Fig. 4. As can be observed, now the Main PA load modulated from half load to full load at the maximum output power, while the Peaking PA load ranges from an open to the optimum impedance value.

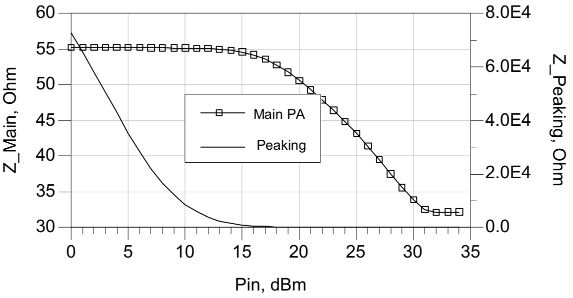


Fig. 4: Simulated load modulations of the Main and Peaking PA of the uneven Doherty amplifier.

The simulated output fundamental voltage amplitudes are reported in Fig. 5, from which it can be observed that the Main PA maintained nearly constant output voltage up to the 6 dB back off, as required in ideal Doherty operation [1].

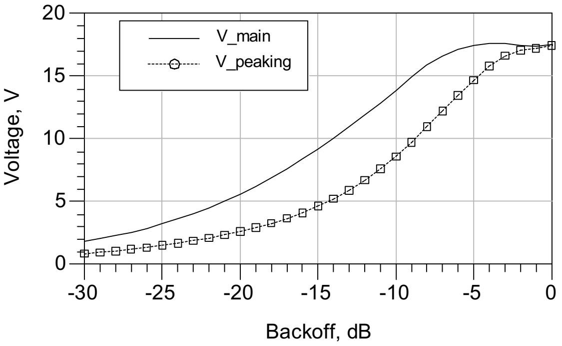


Fig. 5: Simulated fundamental output voltages of the Main and Peaking PA of the uneven Doherty amplifier.

IV. REALIZATION AND EXPERIMENTAL RESULTS

The photo of the uneven Doherty PA is shown in Fig. 6, realised on a PTFE substrate (ε_r=6.15, h=0.635 mm).

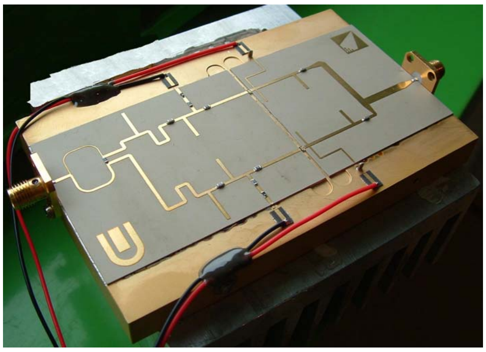


Fig. 6: The fabricated Doherty PA.

The amplifier has been characterized in small signal condition, at the design nominal bias conditions, resulting in V_{DS_Main}=18V, V_{GS_Main}=-4.4V, $V_{DS\_Peaking}$=18V, $V_{GS\_,Peaking}$=-6.5V. The measured reflection and transmission coefficients of the amplifier are shown in Fig. 7.

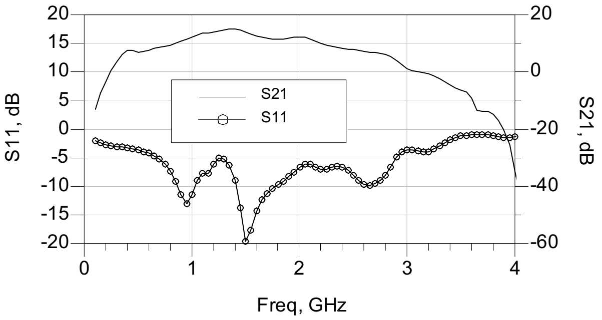


Fig. 7: Measured reflection and transmission coefficients of the Doherty PA.

From S-parameter measurement, a frequency shift for the operating frequency has been observed, resulting in actual 2.0 GHz. Therefore in order to quantify the Doherty large signal performances, several power sweep measurements were performed at 2.0 GHz by tuning the Peaking amplifier bias points.

The obtained measurements are reported in Fig. 8.

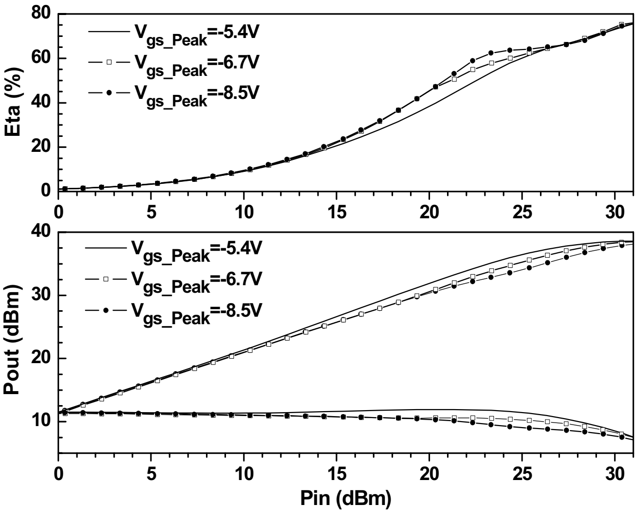


Fig. 8: Measured output power, gain and efficiency performance for different Peaking amplifier biasing condition.

It can be observed that the optimum Doherty operation is found for a Peaking device bias condition of $V_{GS,Peaking}$=-8.5V. In fact, for this biasing condition the Doherty PA maintains a constant efficiency for the upper 6 dB of input power swing.

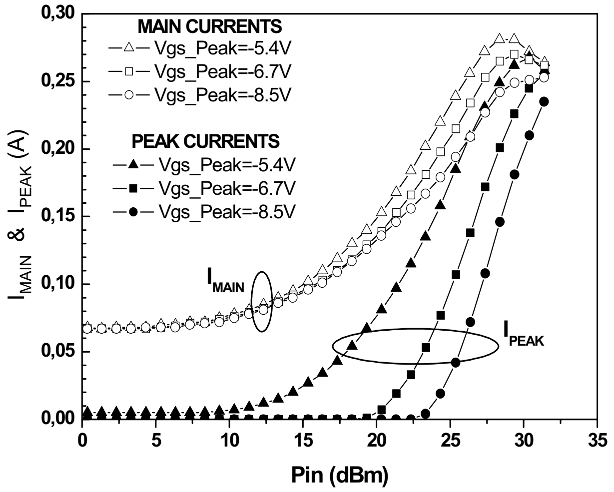


Fig. 9: Measured DC current of Main and Peaking active devices.

The maximum output power measured was 38 dBm, with a power added (or drain) efficiency of 60% (76%). An average value for PAE (drain efficiency) as higher as 52% (62%) and 42% (45%) at the 6 dB and 10 dB back-offs respectively are also achieved.

To clarify the experimental results, the absorbed DC bias current measured for the Main and the Peaking active devices are shown in Fig. 9. It can be observed that the Peaking amplifier turn on properly only for $V_{GS,Peaking}$=-8.5V.

V. CONCLUSIONS

A 6W asymmetrical Doherty amplifier based on GaN technology has been designed. The measured maximum output power of the realised uneven Doherty is 38dBm with 60% of peak power added efficiency (76% of drain efficiency). The power added (drain) efficiency is higher than 52% (62%) up to 6 dB of back off, or 42% (45%) up to 10 dB of back off.

ACKNOWLEDGMENT

This research was performed in the context of the network TARGET "Top Amplifier Research Groups in a European Team" and supported by the Information Society Technologies Programme of the EU under contract IST-1-507893-NOE, www.target-net.org.

REFERENCES

[1] S. C. Cripps, "RF Power Amplfier s for Wirless Communications," Norwood, MA, Artech House, 2006.

[2] F. H. Raab, P. Asbeck, S. C. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, amd N. O. Sokal, "Power Amplifiers and Transmitters for RF and Microwave," IEEE Trans. on MTT, Vol. 50, pp. 814 – 826, Mar. 2002.

[3] W. H. Doherty, "A New High Efficiency Power Amplifier for Modulated Waves," Proc. of the IRE, Vol. 24, pp. 1163 – 1182, 1936.

[4] I. Takenaka, K. Ishikura, H. Takahashi, K. Hasegawa, T. Ueda, T. Kurihara, K. Asano, and N. Iwata, "A Distortion-Cancelled Doherty High Power Amplifier Using 28-V GaAs Hetrojunction FETs for WCDMA Base stations," IEEE Trans. on MTT, Vol. 54, pp. 4513 – 4521, Dec. 2006.

[5] J. R. Gajadharsing, O. Bosma, and P. van Westen, "Analysis and Design of a 200W LDMOS Based Doherty Amplifier for 3G Base Stations," IEEE MTT-S Int. Microwave Symp. Dig., pp. 529–532, 2004.

[6] K-J. Cho, J-H. Kim, and S. P. Stapleton, "A Highly Efficient Doherty Feed-Forward Linear Power Amplifier for W-CDMA Base-Station Applications," IEEE Trans. on MTT, Vol. 53, pp. 292 - 300, Jan. 2005.

[7] J. Lees, M. Goss, J. Benedikt, and P. J. Tasker, "Experimental GaN Doherty Amplifier," Electronics Letters Vol. 41 pp.1284-1285. Nov. 2005.

[8] M. Iwamoto, A. Williams, C. Pin-Fan, A. G. Metzger, L. E Larson, and P. M. Asbeck, "An Extended Doherty Amplifier with High Efficiency Over a Wide Power Range," IEEE Trans. on MTT, Vol. 49, pp. 2472 – 2479, Dec. 2001.

[9] J. Lees, M. Goss, J. Benedikt, and P. J. Tasker, "Single Tone Optimisation of an Adaptive Bias Doherty Structure," IEEE MTT-S Int. Microwave Symp. Dig., pp. 2213–2216, 2003.

[10] J. Kim, J. Cha, I. Kim, and B. Kim, "Optimum Operation of Asymmetrical-Cells-Based Linear Doherty Power Amplifier-Uneven Power Drive and Power Matching," IEEE Trans. on MTT, Vol. 53, pp. 1802 -1809, May 2005.

[11] H. Oraizi and A-R. Sharifi, "Design and Optimisation of Broadband Asymmetrical Multi-Section Wilkinson Power Divider," IEEE Trans. on MTT, Vol. 54, pp. 2220- 2231, May 2006.